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EXAMINER	
BAUER, SCOTT ALLEN	
ART UNIT	PAPER NUMBER
2836	

NOTIFICATION DATE	DELIVERY MODE
11/29/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/811,031	JIN ET AL.	
	Examiner	Art Unit	
	SCOTT BAUER	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-11,13-19,21-26,28-32 and 34-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,8-11,13,16-19,21,24-26,28,31,32,34,37 and 38* is/are rejected.

7)☒ Claim(s) *6,7,14,15,22,23,29,30,35 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-3, 5, 8-11, 13, 16, 37 & 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jenkins et al. (US 6,738,248) in view of Smith (US 5,726844) and Rutfors (WO 02/05380).

With regard to Claim 1, Jenkins et al., in Figure 1, discloses a low noise amplifier (100), comprising: an input (104); and an electrostatic discharge protection circuit including (108), a pair of diodes (D1 & D2) each having a first and a second terminal; a first diode (D1) of the pair having a first terminal coupled to the radio frequency input (104) and a second terminal directly coupled to a first supply (VSS); a second diode (D2) of the pair having a second terminal coupled to the radio frequency input (104) and a first terminal directly coupled to the first supply (VSS); the electrostatic discharge protection circuit is operable to shunt electrostatic discharge current during positive and negative electrostatic discharge events away from the radio frequency input and through the first supply (column 3 lines 34-53).

Jenkins et al. does not teach that the input in a radio frequency input, or that a separate electrostatic discharge clamp is directly coupled between a second voltage supply and the first supply so as to provide a discharge path between the second supply and the first supply during an electrostatic discharge event or that current is discharged away from the radio frequency input to the second supply using the second diode for a positive ESD event or to the second supply using the first diode during a negative ESD event.

Rutfors et al., in fig. 7 teaches a low noise amplifier (335) coupled to a radio frequency input.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jenkins et al. with Rutfors, by incorporating the protection of Jenkins into the device of Rutfors et al., for the purpose of providing ESD protection to a wireless circuit thus preventing the LNA from being damaged.

Further, It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from the prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham, 2 USPQ2d 1647 (1987).*

Smith, in Fig. 1 teaches a device that protects a circuits from ESD events on an input pad (12). Like Jenkins, Smith teaches coupling the input pad to a first power source (Vss) using a first diode (14) and a second diode (16). A positive ESD event is conducted to Vss through diode (16) and a negative diode is conducted to Vss through

the other diode (14). Jenkins further teaches that a separate electrostatic discharge clamp (18) is directly coupled between a second voltage supply (Vdd) and the first supply (Vss) so as to provide a discharge path between the second supply and the first supply during an electrostatic discharge event and that current is discharged away from the input (12) to the second supply (Vdd) using the second diode (16) for a positive ESD event (path 105) and to the second supply (Vdd) using the first diode (14) during a negative ESD event (path 106) (column 3 line 40-column 4 line 43). It is noted that Smith further teaches that zener diode 19 can be omitted such that all currents shunted to Vdd would travel through diodes 14, 16 & 18.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jenkins et al. with Smith, by placing a bi-directional clamp between the terminals VDD and VSS of Jenkins et al., for the purpose of providing bidirectional protection to the buffer (102) from ESD occurring from the power supply for very high and very lower ESD events and to ensure that the voltage between the power rails does not rise too high and thus further damaging circuitry.

With regard to Claim 9, Jenkins et al., in Figure 1, discloses a low noise amplifier (100), comprising: receiving means for receiving an RF input (104); and shunting means (108) including, a pair of diode means (D1 & D2) each having a first terminal and a second terminal; a first diode means (D1) of the pair having a first terminal coupled to the receiving means and a second terminal directly coupled to a first supply; a second

diode means (D2) of the pair having a second terminal coupled to the receiving means and a first terminal coupled directly to the first supply; and the shunting means for shunting electrostatic discharge current during positive and negative electrostatic discharge events away from the receiving means and through the first supply (VSS) (column 3 lines 34-53).

Jenkins et al. does not teach that the input in a radio frequency input, or that a separate electrostatic discharge clamp is directly coupled between a second voltage supply and the first supply so as to provide a discharge path between the second supply and the first supply during an electrostatic discharge event or that current is discharged away from the radio frequency input to the second supply using the second diode for a positive ESD event or to the second supply using the first diode during a negative ESD event.

Rutfors et al., in fig. 7 teaches a low noise amplifier (335) coupled to a radio frequency input.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jenkins et al. with Rutfors, by incorporating the protection of Jenkins into the device of Rutfors et al., for the purpose of providing ESD protection to a wireless circuit thus preventing the LNA from being damaged.

Further, It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed

apparatus from the prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham, 2 USPQ2d 1647 (1987).*

Smith, in Fig. 1 teaches a device that protects a circuits from ESD events on an input pad (12). Like Jenkins, Smith teaches coupling the input pad to a first power source (Vss) using a first diode (14) and a second diode (16). A positive ESD event is conducted to Vss through diode (16) and a negative diode is conducted to Vss through the other diode (14). Jenkins further teaches that a separate electrostatic discharge clamp (18) is directly coupled between a second voltage supply (Vdd) and the first supply (Vss) so as to provide a discharge path between the second supply and the first supply during an electrostatic discharge event and that current is discharged away from the input (12) to the second supply (Vdd) using the second diode (16) for a positive ESD event (path 105) and to the second supply (Vdd) using the first diode (14) during a negative ESD event (path 106) (column 3 line 40-column 4 line 43). It is noted that Smith further teaches that zener diode 19 can be omitted such that all currents shunted to Vdd would travel through diodes 14, 16 & 18.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jenkins et al. with Smith, by placing a bi-directional clamp between the terminals VDD and VSS of Jenkins et al., for the purpose of providing bidirectional protection to the buffer (102) from ESD occurring from the power supply for very high and very lower ESD events and to ensure that the voltage between the power rails does not rise too high and thus further damaging circuitry.

With regard to Claims 2 & 10, Jenkins et al. in view of Smith and Rutfors et al. discloses the low noise amplifier of Claims 1 & 9 wherein the first and second diodes are formed by one of polymer devices and metal oxide silicon devices. (column 3, lines 27-33).

With regard to Claims 3 &11 Jenkins et al. in view of Smith and Rutfors et al., in Figure 1, discloses the low noise amplifier of Claims 1 & 9, wherein the first supply is one of a low voltage supply and a high voltage supply, and if the first supply is a low voltage, then the electrostatic discharge protection circuit is not directly coupled to a corresponding high voltage supply, if the first supply is a high voltage supply, then the electrostatic discharge protection circuit is not directly coupled to a corresponding low voltage supply.

With regard to Claims 5 & 13, Jenkins et al. in view of Smith and Rutfors et al., in Figure 1, discloses the low noise amplifier of Claims 3 & 11 wherein the positive and negative electrostatic discharge events necessarily include a radio frequency input to high voltage supply positive discharge pulse, a radio frequency input to high voltage supply negative discharge pulse, a radio frequency input to low voltage supply positive discharge pulse, and a radio frequency input to low voltage supply negative discharge pulse.

With regard to Claims 8 & 16, Jenkins et al. in view of Smith and Rutfors et al. teaches the low noise amplifier of Claims 1 & 9. Jenkins et al. further teaches that the system is used in a high-speed communication circuit (column 2 lines 37-40). Rutfors et al. also teaches that the system is a wireless system.

Jenkins et al. does not teach that the low noise amplifier is compliant with an IEEE standard selected from the group consisting of 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, and 802.11i, and 802.14.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that a device used in a high speed communication circuit would necessarily be compliant with IEEE standards as the interference created by the device would prevent components that the device relies upon from working properly and to enable the high speed communication circuit to operate and comply with standard industry-wide safety requirements.

With regard to claims 37 & 38, Jenkins in view of Smith and Rutfors discloses the device of claim 1, and further discloses that the electrostatic discharge protection circuit is operable to: shunt electrostatic discharge current during the positive electrostatic discharge (path 109) event away from the radio frequency input (12) to the first supply using the second diode (16), or from the radio frequency input (12) to the second supply (Vdd) using the second diode (16) and the separate electrostatic discharge clamp (18) (path 105) and wherein the electrostatic discharge protection circuit is operable to: shunt electrostatic discharge current during a negative electrostatic discharge event (path

108) away from the radio frequency input (12) to the first supply (Vss) using the first diode (14), or from the radio frequency input (12) to the second supply (Vdd) using the first diode (14) and the separate electrostatic discharge clamp (18) (path 106).

2. Claims 17-19, 21, 24-26, 28, 31, 32 & 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jenkins in view of Smith.

With regard to Claim 17, Jenkins et al., in Figure 1, discloses an electrostatic discharge protection circuit (300), comprising: a pair of diodes (D1 & D2) each having a first terminal and a second terminal; a first diode (D1) of the pair having a first terminal coupled to an input/output pad and a second terminal directly coupled to a first supply; a second diode (D2) of the pair having a second terminal coupled to the input/output pad (104) and a first terminal directly coupled to the first supply; and the electrostatic discharge protection circuit operable to shunt electrostatic discharge current during positive and negative electrostatic discharge events (column 1 lines 36-39).

Jenkins et al. does not teach a separate electrostatic discharge clamp is directly coupled between a second voltage supply and the first supply so as to provide a discharge path between the second supply and the first supply during an electrostatic discharge event or that current is discharged away from the radio frequency input to the second supply using the second diode for a positive ESD event or to the second supply using the first diode during a negative ESD event.

Smith, in Fig. 1 teaches a device that protects a circuits from ESD events on an input pad (12). Like Jenkins, Smith teaches coupling the input pad to a first power source (Vss) using a first diode (14) and a second diode (16). A positive ESD event is conducted to Vss through diode (16) and a negative diode is conducted to Vss through the other diode (14). Jenkins further teaches that a separate electrostatic discharge clamp (18) is directly coupled between a second voltage supply (Vdd) and the first supply (Vss) so as to provide a discharge path between the second supply and the first supply during an electrostatic discharge event and that current is discharged away from the input (12) to the second supply (Vdd) using the second diode (16) for a positive ESD event (path 105) and to the second supply (Vdd) using the first diode (14) during a negative ESD event (path 106) (column 3 line 40-column 4 line 43). It is noted that Smith further teaches that zener diode 19 can be omitted such that all currents shunted to Vdd would travel through diodes 14, 16 & 18.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jenkins et al. with Smith, by placing a bi-directional clamp between the terminals VDD and VSS of Jenkins et al., for the purpose of providing bidirectional protection to the buffer (102) from ESD occurring from the power supply for very high and very lower ESD events and to ensure that the voltage between the power rails does not rise too high and thus further damaging circuitry.

With regard to Claim 24, Jenkins et al., in Figure 1, discloses an electrostatic discharge protection circuit (300) for discharging electrostatic discharge events, comprising: shunting means (108) including, a pair of diode means having a first terminal and a second terminal; a first diode means (D1) of the pair having a first terminal directly coupled to an input/output pad (104) a second terminal coupled to a first supply; and a second diode means (D2) of the pair having a second terminal coupled to the input/output pad and a first terminal directly coupled to the first supply; and the shunting means for shunting electrostatic discharge current during positive and negative electrostatic discharge events.

Jenkins et al. does not teach a separate electrostatic discharge clamp is directly coupled between a second voltage supply and the first supply so as to provide a discharge path between the second supply and the first supply during an electrostatic discharge event or that current is discharged away from the radio frequency input to the second supply using the second diode for a positive ESD event or to the second supply using the first diode during a negative ESD event.

Smith, in Fig. 1 teaches a device that protects a circuits from ESD events on an input pad (12). Like Jenkins, Smith teaches coupling the input pad to a first power source (Vss) using a first diode (14) and a second diode (16). A positive ESD event is conducted to Vss through diode (16) and a negative diode is conducted to Vss through the other diode (14). Jenkins further teaches that a separate electrostatic discharge clamp (18) is directly coupled between a second voltage supply (Vdd) and the first supply (Vss) so as to provide a discharge path between the second supply and the first

supply during an electrostatic discharge event and that current is discharged away from the input (12) to the second supply (Vdd) using the second diode (16) for a positive ESD event (path 105) and to the second supply (Vdd) using the first diode (14) during a negative ESD event (path 106) (column 3 line 40-column 4 line 43). It is noted that Smith further teaches that zener diode 19 can be omitted such that all currents shunted to Vdd would travel through diodes 14, 16 & 18.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jenkins et al. with Smith, by placing a bi-directional clamp between the terminals VDD and VSS of Jenkins et al., for the purpose of providing bidirectional protection to the buffer (102) from ESD occurring from the power supply for very high and very lower ESD events and to ensure that the voltage between the power rails does not rise too high and thus further damaging circuitry.

With regard to Claim 31, Jenkins et al., in Figure 1, discloses a method for discharging electrostatic discharge, comprising: providing a first direct discharge path between an input/output pad and a first supply; providing a second direct discharge path between the input/output pad and the first supply; and shunting electrostatic discharge current during positive and negative electrostatic discharge events through one of the first discharge path and the second discharge path.

Jenkins et al. does not teach providing a third discharge path between the first supply and a second supply during an electrostatic discharge event and shunting ESD

current during a positive ESD event. away from the input/output pad to the first supply using the second direct discharge path and to the second supply using the second direct discharge path and the third direct discharge path, and during a negative electrostatic discharge event away from the input/output pad to the first supply using the first direct discharge path and to the second supply using the first direct discharge path and the third direct discharge path.

Jenkins et al. does not teach a separate electrostatic discharge clamp is directly coupled between a second voltage supply and the first supply so as to provide a discharge path between the second supply and the first supply during an electrostatic discharge event or that current is discharged away from the radio frequency input to the second supply using the second diode for a positive ESD event or to the second supply using the first diode during a negative ESD event.

Smith, in Fig. 1 teaches a device that protects a circuits from ESD events on an input pad (12). Like Jenkins, Smith teaches coupling the input pad to a first power source (Vss) using a first diode (14) and a second diode (16). A positive ESD event is conducted to Vss through diode (16) and a negative diode is conducted to Vss through the other diode (14). Jenkins further teaches that a separate electrostatic discharge clamp (18) is directly coupled between a second voltage supply (Vdd) and the first supply (Vss) so as to provide a discharge path between the second supply and the first supply during an electrostatic discharge event and that current is discharged away from the input (12) to the second supply (Vdd) using the second diode (16) for a positive ESD event (path 105) and to the second supply (Vdd) using the first diode (14) during a

negative ESD event (path 106) (column 3 line 40-column 4 line 43). It is noted that Smith further teaches that zener diode 19 can be omitted such that all currents shunted to Vdd would travel through diodes 14, 16 & 18.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jenkins et al. with Smith, by placing a bi-directional clamp between the terminals VDD and VSS of Jenkins et al., for the purpose of providing bidirectional protection to the buffer (102) from ESD occurring from the power supply for very high and very lower ESD events and to ensure that the voltage between the power rails does not rise too high and thus further damaging circuitry.

With regard to Claims 18, & 25, Jenkins et al. in view of Duclos discloses the low noise amplifier of Claims 24 & 31, wherein the first and second diodes are formed by one of polymer devices and metal oxide silicon devices (column 3, lines 27-33).

With regard to Claims 19, 26 & 32, Jenkins et al. in view of Smith, in Figure 1, discloses the low noise amplifier of Claims 17, 24 & 31, wherein the first supply is one of a low voltage supply and a high voltage supply, and if the first supply is a low voltage, then the electrostatic discharge protection circuit is not directly coupled to a corresponding high voltage supply, if the first supply is a high voltage supply, then the

electrostatic discharge protection circuit is not directly coupled to a corresponding low voltage supply.

With regard to Claims 21, 28 & 34, Jenkins et al. in view of Smith, in Figure 1, discloses the low noise amplifier of Claims 19, 26 & 32 wherein the positive and negative electrostatic discharge events necessarily include a radio frequency input to high voltage supply positive discharge pulse, a radio frequency input to high voltage supply negative discharge pulse, a radio frequency input to low voltage supply positive discharge pulse, and a radio frequency input to low voltage supply negative discharge pulse.

Allowable Subject Matter

Claims 6, 7, 14, 15, 22, 23, 29, 30, 35 & 36 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 6 & 14, would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims because the prior art of record does not teach or fairly suggest an apparatus comprising all the features as recited in the claims and in combination with the low voltage supply floating during the radio frequency input to high voltage supply positive discharge pulse and the radio frequency input to high voltage supply negative discharge pulse.

Claims 7 & 15 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims because the prior art of record does not teach or fairly suggest an apparatus comprising all the features as recited in the claims and in combination with the high voltage supply floating during the radio frequency input to low voltage supply positive discharge pulse and the radio frequency input to low voltage supply negative discharge pulse.

Claims 22, 29 & 35 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims because the prior art of record does not teach or fairly suggest a low noise amplifier comprising all the features as recited in the claims and in combination with wherein the low voltage supply floating during the radio frequency input to high voltage supply positive discharge pulse and the radio frequency input to high voltage supply negative discharge pulse.

Claims 23, 30 & 36 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims because the prior art of record does not teach or fairly suggest a low noise amplifier comprising all the features as recited in the claims and in combination with the high voltage supply necessarily floats during the radio frequency input to low voltage supply positive discharge pulse and the radio frequency input to low voltage supply negative discharge pulse.

Response to Arguments

3. Applicant's arguments with respect to claims 1-3, 5, 8-11, 13, 16-19, 21, 24-26, 28, 31, 32, 37 & 38 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's amendments are related to the various discharge paths of Applicant's invention. The Smith reference has been introduced to teach the various ESD discharge paths between two diodes coupled between an input pad and ground and a clamp coupled between power and ground. Smith teaches that the diode (19) can be omitted thus creating a circuit similar to Applicant's invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SCOTT BAUER whose telephone number is 571-272-5986. The examiner can normally be reached on M-F 9am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jared Fureman can be reached on 571-272-2391. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SAB/
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/Jared J. Fureman/
Supervisory Patent Examiner, Art Unit 2836